2.   Claims 1-5, and 9 have been rejected under 35 USC §
102 (b) as being anticipated by Ciccone (U.S. Patent No.
5,917,255).   In particular, the Examiner stated that,
"Ciccone discloses in figure 3 an apparatus for providing a
method of enabling an IC, the method comprises steps of
establishing an idle state that holds a portion of the IC
in a reset condition when a power source is operably
coupled to the IC (col. 1, lines 12-16 and col. 3, lines
12-27); receiving a power enable signal (MANUAL); enabling,
in response to the power enable signal, an on-chip power
converter (transistors PWK and PMAM) of the IC to generate
one supply (POEDC) from a power source (Vps); and when the
one supply has reached a steady-state (col. 1, lines 61-67,
col. 2 lines 1-5), enabling functionality of the IC as
required by claim 1.   The applicant respectfully disagrees
with the Examiner's characterization of the present claim
in view of the cited prior art.

The method of claim 1 has four steps:

a)   establishing an idle state that holds at least a
portion of the stand-alone IC in a reset condition when a
power source is operably coupled to the stand-alone IC;

b)   receiving a power enable signal;

c)   enabling, in response to the power enable signal, an
on-chip power converter of the stand-alone IC to generate
at least one supply from the power source; and

d)   when the at least one supply has substantially reached
a steady-state condition, enabling functionality of the
stand-alone IC.

The specification of the present patent application
teaches that a power source may be a battery, solar power
generator, or other power source that produces a voltage
that is not the proper voltage for powering at least a
portion of the stand-alone integrated circuit 10. (page 3,
line 5 and lines 16 - 18). Ciccone does not teach or
suggest having a power source (e.g., a battery) coupled to
the IC, where the power source does not produce the desired
voltage for supplying the IC. The passages of Ciccone
cited by the Examiner relate to the power supply voltage
(Vps), which is used to source power to the IC. While not
specifically stated by Ciccone, but implied, the power
supply voltage (Vps) is generated by a power supply, which,
as is known in the art, converts a source voltage, or
current, into a desired output voltage. As such, the power
source of the present claim is not the power supply as
taught by Ciccone.

Further, Ciccone teaches, as shown in Figures 1 - 3
and as described in the corresponding text, a reset signal
is generated that resets the IC when the supply voltage
reaches a certain threshold and after a delay time interval
has expired. (See specifically column 3, lines 41 - 47.)
As such, Ciccone teaches resetting the IC after the supply
voltage has reached a predetermined level and after a delay
time period has expired. Step (a) of the present claim
holds at least a portion of the IC in a reset condition

when a power source (e.g., a battery) is coupled to the IC, but prior to the generation of the power supply voltage.

Still further, Ciccone does not teach or suggest enabling an on-chip power converter to generate at least one supply from the power source in response to the power enable signal. While Ciccone teaches a power enable signal (i.e., MANUAL), this signal does not enable the generation of a supply voltage by an on-chip power converter. As shown in figure 3 and as described in the corresponding text, Ciccone teaches that the MANUAL signal is used to activate the voltage level detector. Transistors PWK and PMAN do not provide a supply voltage to the IC, but function as switches to enable the voltage level detector.

Even further, the present claim includes enabling functionality of the IC when the at least one supply has substantially reached a steady-state condition. In contrast, Ciccone teaches that the IC is placed in a reset condition when the supply voltage reaches a predetermined value.

Therefore, it is clear that the power on reset circuit of Ciccone does not teach or suggest the enabling sequence of a stand alone IC as claimed in claim 1. In particular, the present claim includes two power elements: the power source and the on-chip power converter, Ciccone only includes one power element: the power supply that generates the power supply signal. Further, the present claim places at least a portion of the IC in a reset condition when the power source is coupled to the IC, but before the power converter generates the supply voltage and, once the supply

voltage is generated, the functionality of the IC is enabled. In contrast, Ciccone generates the reset signal, which places the IC in reset, after the supply voltage is generated.

Based on the foregoing discussion, the applicant believes that claim 1 overcomes the present rejection.

2. Claims 2 - 5, and 9 are dependent upon claim 1, which has been shown to overcome the present rejection. Since each of claims 2 - 5, and 9 introduce additional patentable subject matter, especially when viewed in context with claim 1, the applicant believes that claims 2 - 5, and 9 also overcome the present rejection.

3.   For the foregoing reasons, the applicant believes that claims 1 - 9 are in condition for allowance and respectfully request that they be passed to allowance. The applicant appreciates the allowance of claims 10 - 22.

4.   The Examiner is invited to contact the undersigned by telephone or facsimile if the Examiner believes that such a communication would advance the prosecution of the present invention.
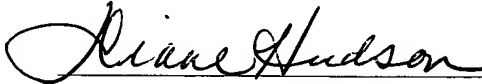
RESPECTFULLY SUBMITTED,

By: _____
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CERTIFICATE OF MAILING
37 C.F.R 1.8

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, DC 20231, on the date below:

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